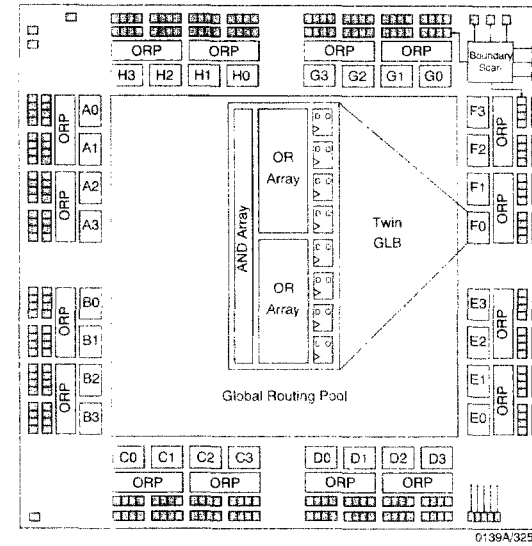
ispLSI® 3256E

High Density Programmable Logic

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **256 I/O Pins**
  - **12000 PLD Gates**
  - **512 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **fmax = 100 MHz Maximum Operating Frequency**
  - **tpd = 10 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **5V In-System Programmable (ISP™) using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Five Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 3256E is a High Density Programmable Logic Device containing 512 Registers, 256 Universal I/O pins, five Dedicated Clock Input Pins, 16 Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3256E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3256E device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3 There are a total of 32 Twin GLBs in the ispLSI 3256E device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

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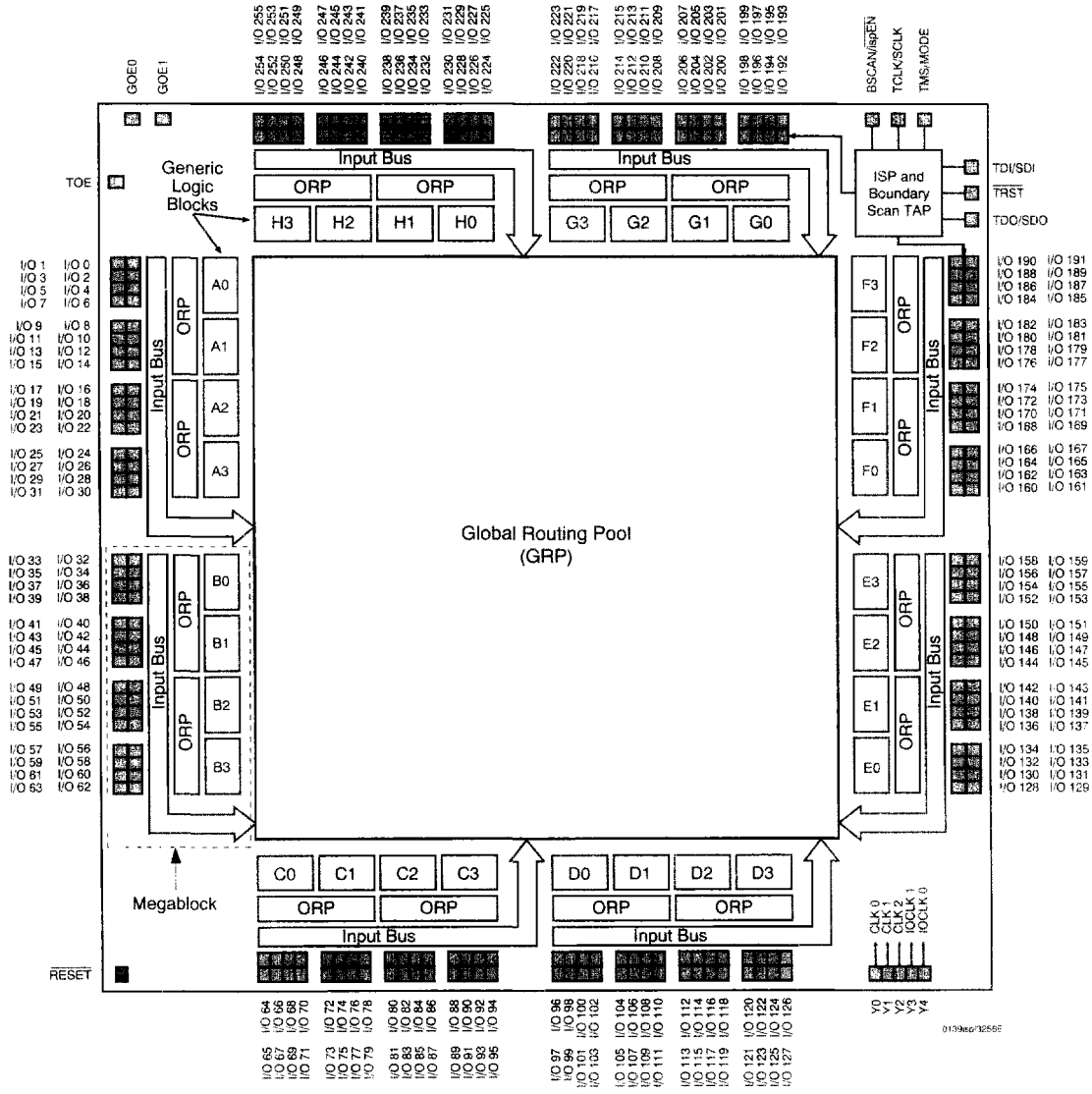
Functional Block Diagram

Figure 1. ispLSI 3256E Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 256 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 256 I/O Cells are grouped into 16 sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the ORP. The ispLSI 3256E device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3256E device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3256E is its Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3256E supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3256E

Attribute	Quantity
Twin GLBs	32
Registers	512
I/O Pins	256
Global Clocks	5
Global OE	2
Test OE	1

Table - 0030/3256E

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	10.0	—	15.0	ns
tpd2	A	2	Data Propagation Delay	—	13.0	—	18.0	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	100	—	70.0	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	77.0	—	50.0	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	100	—	83.0	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.5	—	9.0	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	6.5	—	9.0	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0.0	—	0.0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.5	—	11.0	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	7.0	—	10.0	ns
th2	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	13.5	—	15.0	ns
trw1	—	13	Ext. Reset Pulse Duration	6.5	—	12.0	—	ns
tptoeen	B	14	Input to Output Enable	—	16.0	—	19.0	ns
tptoedis	C	15	Input to Output Disable	—	16.0	—	19.0	ns
tgoeen	B	16	Global OE Output Enable	—	9.0	—	12.0	ns
tgoedis	C	17	Global OE Output Disable	—	9.0	—	12.0	ns
ttoeen	—	18	Test OE Output Enable	—	12.0	—	15.0	ns
ttoedis	—	19	Test OE Output Disable	—	12.0	—	15.0	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	5.0	—	6.0	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	5.0	—	6.0	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	4.5	—	5.0	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	—	0.0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3256E.eps